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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/652,998	08/31/2000	D. Mark Durcan	98-1068.06	4016

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EXAMINER

MAI, ANH D

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 04/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/652,998

Applicant(s)

DURCAN ET AL.

Examiner

Anh D. Mai

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 December 2001.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 13, 14, 67 and 68 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 13, 14, 67 and 68 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Amendment

The Amendment filed December 21, 2001 was entered as Paper No. 8. Claim 13 was amended; Claims 67 and 68 were added.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 67 and 68 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 67 and 68 recite: “a trench laterally positioned between the second and third bottom electrode to expose a portion of exterior surfaces of the second and third bottom electrodes” on lines 6-7, respectively.

The exterior surface of the *second and third bottom electrodes* have not been *exposed*.

There is at least a capacitor dielectric layer (23C) covering the surfaces, interior and exterior, of the bottom electrode (20), within the trench, at all time. (See Fig. 12).

How can the exterior surfaces of the second and third bottom electrodes be exposed while being covered by at least one layer ?

As best understood by the examiner, the limitation of the claim should read: *a trench laterally positioned between the second and third bottom electrode*.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Becker (U.S. Patent No. 5,770,498).

Becker teaches an array of capacitors substantially similar as claimed including:

a first bottom capacitor plate (44);

a second bottom capacitor plate (44);

a third bottom capacitor plate (44); (not shown);

a contact (54) between the first bottom capacitor plate and the second bottom capacitor plate, the contact downwardly extends from a vertical height above a top of the first bottom capacitor plate (44);

a trench between the second bottom capacitor plate and the third bottom capacitor plate;

a common top capacitor plate (48) over the first bottom capacitor plate (44), the second bottom capacitor plate (44), and the third bottom capacitor plate (44), wherein the top capacitor plate (48) extends toward the contact (34) at a first level within the array, the top capacitor plate (48) includes a lateral clearance opening at the first level around the contact, and wherein the top capacitor plate (48) lines a side of the trench and further lines a bottom of the trench at a second level within the array; and

a dielectric (46) between the top capacitor plate (48) and the first, second, and third bottom capacitor plates (44). (See Fig. 10).

The third bottom capacitor plate (44) is not shown but can be understood as on the outside of the first and second bottom capacitor plate since the capacitors of Becker are formed in an array.

With respect to claim 14, the top capacitor plate (48) extends toward the top of the contact (34).

3. Claims 67 and 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admitted prior art in view of Zahurak (U.S. Patent No. 6,150,211).

With respect to claim 67, as best understood by the examiner, the admitted prior art teaches an array of capacitor substantially similar as claimed including:

first, second and third memory cell capacitors comprising first, second and third bottom container-shaped electrodes (20), respectively;

a bit line contact laterally positioned between the first and second memory cell;

a trench laterally positioned between the second (20) and third (20) bottom electrodes to expose a portion of exterior surfaces of the second and the third bottom electrodes (20);

a common top electrode (24B) capacitively coupled to the first, second and third electrodes via a capacitor dielectric layer (23B); and

a bit line contact insulation region (60B) surrounding the bit line contact and filling a region between the bit line contact and the bottom electrodes (20). (See Figs. 1 and 3).

Thus, the admitted prior art is shown to teach all the features of the claim with the exception of explicitly showing a bit line contact within the contact hole (5).

However, Zahurak teaches a bit line contact (70) formed within the contact hole downwardly extends from a vertical height above a top of the bottom electrode (66) and the top electrode (68) includes a lateral clearance opening around the bit line contact (70). (See Fig. 20).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form a bit line contact within the contact hole (5) of the admitted prior art as taught by Zahurak to electrically connecting the bit line and the source/drain region (14B).

Further, the top electrode (68) of Zahurak has a lateral clearance opening above the top of the bottom electrode and around the bit line (70) to eliminate shortage between the bit line contact (70) and the top electrode (68).

With respect to claim 68, as best understood by the examiner, the admitted prior art teaches an array of capacitor substantially similar as claimed including:

first, second and third memory cell capacitors comprising first, second and third bottom container-shaped electrodes (20), respectively;

a bit line contact site (5) laterally positioned between the first and second memory cell, the bit line contact site downwardly extends from a vertical height above a top of the bottom electrode (20);

a trench laterally positioned between the second and third bottom electrodes (20) to expose a portion of exterior surfaces of the second and the third bottom electrodes (20);

a common top electrode (24B) capacitively coupled to the first, second and third electrodes via a capacitor dielectric layer (23B); and

a bit line contact insulation region (60B) surrounding the bit line contact and filling a region between the bit line contact and the first and second bottom electrodes (20), wherein the bit line contact insulation region (60B) prevents the top electrode (24B) from downwardly extending between the bit line contact and the first and second bottom electrodes (20).

Thus, the admitted prior art is shown to teach all the features of the claim with the exception of explicitly showing a bit line contact within the contact site (5).

However, Zahurak teaches a bit line contact (70) formed within the contact hole downwardly extends from a vertical height above a top of the bottom electrode (66) and the top electrode (68), wherein the top electrode (68) includes a lateral clearance opening around the bit line contact (70). (See Fig. 20).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form a bit line contact within the contact site (5) of the admitted prior art as taught by Zahurak to electrically connecting the bit line and the source/drain region (14B).

Further, the top electrode (68) of Zahurak has a lateral clearance opening above the top of the bottom electrode and around the bit line (70) to eliminate shortage between the bit line contact (70) and the top electrode (68).

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Response to Arguments

4. Applicant's arguments with respect to claims 13 and 14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the

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organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
April 16, 2002


OLIK CHAUDHURI
SUPERVISORY PATENT EXAMINER
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